2814

Docket: 14466

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	John Snyder		
Application No.:	09/928,124		
Filing Date:	August 10, 2001	Examiner:	L. Pham
Title:	**A FABRICATION METHOD FOR A DEVICE FOR REGULATING FLOW OF ELECTRIC CURRENT WITH HIGH DIELECTRIC CONSTANT GATE INSULATING LAYER AND SOURCE/DRAIN FORMING SCHOTTKY CONTACT OR SCHOTTKY-LIKE REGION WITH SUBSTRATE**	Group Art Unit:	2814

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this document is being sent via First Class U.S. mail addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23 day of June, 2003.

KrisAnne Popovits

Dear Sir:

The following documents are enclosed in connection with the above-referenced patent application:

1. Information Disclosure Statement Under 37 CFR 1.97(c) (2 pages);
2. Form PTO/SB/08A (6 pages, submitted in duplicate);
3. Copies of 65 References Cited;
4. Fee Determination (After Amendment of Claims) (1 page);
5. Check No. 956872 in the amount of $180; and
6. Return Receipt Postcard.

612-340-7990

Devan Tadma Nabhan

Respectfully submitted,

DORSEY & WHITNEY LLP
Customer Number 25763

Date: 6.23.03

By:

Jason R. Kraus (Reg. No. 42,765)
Intellectual Property Department
Suite 1500, 50 South Sixth Street
Minneapolis, MN 55402-1498
(612) 340-5617
612-340-2600

FEE DETERMINATION (After Amendment of Claims)

	Complete if Known
Application No.	09/928,124
Filing Date	August 10, 2001
First Named Inventor	John Snyder
Group Art Unit	2814
Examiner Name	L. Pham
Atty. Docket Number	14466
Claims as Amended in Response to Office Action dated:	N/A

METHOD OF PAYMENT (Check One)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
   Deposit Account No.: 04-1420
   Deposit Account Name: DORSEY & WHITNEY LLP
   ☒ Charge any additional fee required under 37 C.F.R. 1.16 and 1.17
   ☒ Applicant claims small entity status (see 37 C.F.R. 1.27)
2. ☒ Check Enclosed

AMENDMENT FEE CALCULATION

1. EXTRA* CLAIM FEES

	Claims Remaining after Amendment		Highest Number Previously Paid for		Present Extra		Fee from Below*		Additional Fee
Total		-		=		x		=	
Indep.		-		=		x		=	
First Presentation of Multiple Dependent Claim						x		=	
							Subtotal (1)		

*Calculation of Extra Claim Fees

Large Entity Fee	Small Entity Fee	Fee Description
18	9	Claims in excess of 20
84	42	Independent claims in excess of 3
280	140	Multiple dependent Claim
84	42	Reissue independent claims over original patent
18	9	Reissue claims in excess of 20 and over original patent

AMENDMENT FEE CALCULATION (Continued)

3. ADDITIONAL FEES

Large Entity Fee	Small Entity Fee	Fee Description	Fee Paid
110	55	Extension for reply within first month	
410	205	Extension for reply within second month	
930	465	Extension for reply within third month	
1,450	725	Extension for reply within fourth month	
1,970	985	Extension for reply within fifth month	
1,300	650	Issue Fee-Utility/Reissue	
320	160	Notice of Appeal	
320	160	Filing brief in support of appeal	
280	140	Request for oral hearing	
110	55	Terminal Disclaimer Fee	
110	55	Petition to revive – unavoidable	
1,300	650	Petition to revive – unintentional	
130	130	Petitions to the Commissioner	
180	180	Submission of IDS	$180.00
750	375	Request for Continued Examination (RCE)	

Other fee (specify):

Subtotal (2) $180.00

Total Amount of Payment: $180.00

Submitted by:

CUSTOMER NUMBER	
25763	DORSEY & WHITNEY LLP Intellectual Property Department 50 South Sixth Street, Suite 1500 Minneapolis, MN 55402-1498

Name: Jason R. Kraus	Reg. No.: 42,765	Telephone: (612) 340-5617	Facsimile: (612) 340-8856
Signature:			Date: 6-23-03

Docket: 14466

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INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(c)

Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this document is being sent via First Class U.S. mail addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23 day of June, 2003.

KrisAnne Popovits

Dear Sir:

Pursuant to 37 CFR § 1.97(c), the references listed on the attached Form PTO/SB/08A (7 sheets, submitted in duplicate) are brought to the attention of the Examiner for consideration in connection with the examination of the above-identified patent application. Copies of the identified references are enclosed as necessary. This Information Disclosure Statement ("IDS") is filed on or before the mailing date of a final office action or a notice of allowance is accompanied by the fee set forth in 37 CFR § 1.17(p).

Payment of Fee Under 37 CFR § 1.17(p)

The fee under 37 CFR § 1.17(p), required for submission of an IDS under 37 CFR § 1.97(c), is enclosed, as referenced in the attached Fee Transmittal Sheet.

Pursuant to the Manual of Patent Examining Procedure, Chapter 609, Applicant requests that the Examiner consider each of the listed documents and initial and return to the undersigned a copy of the enclosed PTO/SB/08A (submitted in duplicate).

Respectfully submitted,

DORSEY & WHITNEY LLP
Customer Number 25763

Date: 6.23.03

By: _____

Jason R. Kraus
Reg. No. 42,765
Intellectual Property Department
Suite 1500
50 South Sixth Street
Minneapolis, MN 55402-1498
(612) 340-5617

PTO/SB/08A (10/01) (modified)
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Application Number	**09/928,124**
Filing Date	**August 10, 2001**
First Named Inventor	**John Snyder**
Art Unit	**2814**
Examiner Name	**L. Pham**
Attorney Docket Number	**14466**

Sheet	**1**	**of**	**6**

U.S. PATENT DOCUMENTS

*Examiner Initials	Cite No.	DOCUMENT NUMBER Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 4,053,924	10-11-1977	Roman et al.	
		US- 4,300,152	11-10-1981	Lepselter	
		US- 4,942,441	7-17-1990	Konishi et al.	
		US- 5,040,034	8-13-1991	Murakami et al.	
		US- 5,079,182	1-7-1992	Ilderem et al.	
		US- 5,323,053	6-21-1994	Luryi et al.	
		US- 5,361,225	11-1-1994	Ozawa	
		US- 5,444,302	8-22-1995	Nakajima et al.	
		US- 5,663,584	9-2-1997	Welch	
		US- 5,760,449	6-2-1998	Welch	
		US- 5,767,557	6-16-1998	Kizilyalli	
		US- 5,801,398	9-1-1998	Hebiguchi	

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	FOREIGN PATENT DOCUMENT Country Code:	Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	TRANSLATION YES	TRANSLATION NO
		EP	0 603 102 A2	6-22-1994			☒	☐
		PCT	WO 01/45157 A1	6-21-2001			☐	☐
							☐	☐
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							☐	☐
							☐	☐
							☐	☐

EXAMINER SIGNATURE	DATE CONSIDERED

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Sheet	**2**	**of**	**6**

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		US- 5,883,010	3-16-1999	Merrill et al.	
		US- 6,037,605	3-14-2000	Yoshimura	
		US- 6,160,282	12-12-2000	Merrill	
		US- 6,268,636	7-31-2001	Welch	
		US- 6,323,528	11-27-2001	Yamazaki et al.	
		US- 6,353,251	3-5-2002	Kimura	
		US- 6,420,742	7-16-2002	Ahn et al.	
		US- 6,509,609	1-21-2003	Zhang et al.	
		US- 2001/0024847 A1	9-27-2001	Snyder	
		US- 2002/0030231	3-14-2002	Okawa et al.	
		US-			

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							☐	☐
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							☐	☐
							☐	☐

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Sheet	**3**	**of**	**6**

OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

*Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	TRANSLATION YES	TRANSLATION NO
		LEPSELTER, M.P., SZE, S.M. SB-IGFET: An Insulated Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain. Proceedings of the IEEE, August 1968; pp. 1400-1402.	☐	☐
		LEPSELTER, M.P., MACRAE, A.U., MACDONALD, R.W. SB-IGFET, II: An Ion Implanted IGFET Using Schottky Barriers. Proceedings of the IEEE, May 1969; pp. 812-813.	☐	☐
		KISAKI, Hitoshi. Tunnel Transistor. Proceedings of the IEEE, July 1973; pp. 1053-1054.	☐	☐
		KOENEKE, C.J., SZE, S.M., LEVIN, R.M., KINSBRON, E. Schottky MOSFET for VLSI. *IEDM*, 1981; pp. 367-370.	☐	☐
		SUGINO, M., AKERS, L.A., REBESCHINI, M.E. CMOS Latch-Up Elimination Using Schottky Barrier PMOS. *IEDM*, 1982; pp. 462-465.	☐	☐
		KOENEKE, C.J., LYNCH, W.T. Lightly Doped Schottky MOSFET. *IEDM*, 1982; pp. 466-469.	☐	☐
		MOCHIZUKI, T., WISE, K.D. An n-Channel MOSFET with Schottky Source and Drain. *IEEE Electron Device Letters, EDL-5*, No. 4, April 1984; pp. 108-111.	☐	☐
		OH, C.S., KOH, Y.H., KIM, C.K. A New P-Channel MOSFET Structure with Schottky Clamped Source and Drain, *IEDM*, 1984; pp. 609-612.	☐	☐
		SWIRHUN, Stanley E., et al. A VLSI Suitable Schottky Barrier CMOS Process. *IEEE Transactions on Electron Devices, ED-32*, No. 2, February 1985; pp. 194-202.	☐	☐
		TOVE, P.A., BOHLIN, K., MASSZI, F., NORDE, H., NYLANDER, J., TIREN, T., MAGNUSSON, U. Complementary Si MESFET Concept Using Silicon-on-Sapphire Technology. *IEEE Electron Device Letters*, Vol. 9, No. 1, January 1988; pp. 47-49.	☐	☐
		TOVE, P.A., BOHLIN, K.E., NORDE, H., MAGNUSSON, U., TIREN, J., SODERBARG, A., ROSLING, M., MASSZI, F., NYANDER, J. Silicon IC Technology Using Complementory MESFETs. Solid State Devices, Elsevier Science Publishers (North Holland), 1988; pp. 607-609.	☐	☐

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Sheet	**4**	**of**	**6**

OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

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		TSUI, B., CHEN, M. A Novel Process for High-Performance Schottky Barrier PMOS. *J. Electrochem Soc.*, Vol. 136, No. 5, May 1989; pp. 1456-1459.	☐	☐
		MISRA, D., SIMHADRI, V.S. A Survey of the Potential of an IrSi Schottky Barrier MOSFET Based on Simulation Studies. *Solid State Electronics*, Vol. 35, No. 6, 1992; pp. 829-833.	☐	☐
		HATTORI, Reiji, NAKAE, Akihiro, SHIRAFUJI, Junji. A New Type of Tunnel-Effect Transistor Employing Internal Field Emission of Schottky Barrier Junction. *Japan J. Appl. Phys.*, Vol. 31, 1992; pp. L1467-L1469.	☐	☐
		HATTORI, Reiji, SHIRAFUJI, Junji. Numerical Simulation of Tunnel Effect Transistors. *Japan J. Appl. Phys.*, Vol. 33, 1994; pp. 612-618.	☐	☐
		TUCKER, J.R., WANG, C., LYDING, J.W., SHEN, T.C., ABELN, G.C. Nanometer Scale MOSFETs and STM Patterning on Si. *SSDM 1994*, August 1994; pp. 322-324.	☐	☐
		TUCKER, J.R., WANG, C., CARNEY, P.S. Silicon Field-Effect Transistor Based on Quantum Tunneling. *Applied Physics Letters*, Vol. 65, No. 5, 1 August 1994; pp. 618-620.	☐	☐
		KIMURA, Mitsuteru, MATSUDATE, Tadashi. A New Type of Schottky Tunnel Transistor. *IEEE Electron Device Letters, EDL-15*, No. 10, October 1994, pp. 412-414.	☐	☐
		SNYDER, John P., HELMS, C.R., NISHI, Yoshio. Experimental Investigation of a PtSi Source and Drain Field Emission Transistor. *Applied Physics Letters*, Vol. 67, No. 10, 4 September 1995; pp. 1420-1422.	☐	☐
		WOLF, Stanley. Silicon Processing for the VLSI Era. Volume 3: The Submicron MOSFET, Lattice Press, Sunset Beach, CA, 1995; pp. 523-528.	☐	☐
		ASHTON, S.A., ISMAIL, K., CHU, J.O., CHAN, K. A MOS Transistor with Schottky Source/Drain Contacts and a Self-Aligned Low-Resistance T-gate. *Microelectronics Engineering*, Vol. 35, 1997; pp. 361-363.	☐	☐
		NISHISAKA, Mika, ASANO, Tanemasa. Reduction of the Floating Body Effect in SOI MOSFETs by Using Schottky Source/Drain Contacts. *Japan J. Appl. Phys.*, Vol. 37, March 1998; pp. 1295-1299.	☐	☐

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		WANG, C., SNYDER, John P., TUCKER, J.R. Sub-50nm PtSi Schottky Source/Drain p-MOSFETs. *56th Annual Device Research Conference Digest*, June 1998, pp. 72-73.	☐	☐
		ZHAO, Q.T., KLINKHAMMER, F., DOLLE, M., KAPPIUS, L., MANTL, S. Nanometer Patterning of Epitaxial CoSi2/Si(100) for Ultrashort Channel Schottky Barrier Metal-Oxide-Semiconductor Field Effect Transistors. *Applied Physics Letters*, Vol. 74, No. 3, 18 January 1999; pp. 454-456.	☐	☐
		WANG, C., SNYDER, John P., TUCKER, J.R. Sub-40nm PtSi Schottky Source-Drain Metal-Oxide-Semiconductor Field-Effect-Transistors. *Applied Physics Letters*, Vol. 74, No. 8, 22 February 1999; pp. 1174-1176.	☐	☐
		SNYDER, John P., HOLMS, C.R., NISHI, Yoshio. Analysis of the Potential Distribution in the Channel Region of a Platinum Silicided Source/Drain Metal Oxide Semiconductor Field Effect Transistor. *Applied Physics Letters*, Vol. 74, No. 22, 31 May 1999; pp. 3407-3409.	☐	☐
		SAITOH, W., YAMAGAMI, S., ITOH, A., ASADA, M. 35nm Metal Gate SOI-p-MOSFETs with PtSi Schottky Source/Drain. *57th Annual Device Research Conference Digest*, June 1999; pp. 30-31.	☐	☐
		TUCKER, J.R. Schottky Barrier MOSFETs for Silicon Nano-electronics. *IEEE Frontiers in Electronics*, January 1997; pp. 97-100.	☐	☐
		LAPLANTE, Philip A. (Editer-in-Chief). Comprehensive Dictionary of Electrical Engineering. IEEE Press, 1999, page 97.	☐	☐
		MULLER, Richard S. and KAMINS, Theodore I. Device Electronics for Integrated Circuit. John Wiley & Sons, Second Edition, 1977, 1986, pp. 448, 505-511.	☐	☐
		PIERRET. Modular Series On Solid State Devices, vol. I Semiconductor Fundamentals, Addison-Wesly, 1983; pp. 29-33.	☐	☐
		NEUDECK, Gerold W. Volume II: The PN Junction Diode, Modular Series On Solid State Devices. Addison-Wesley, 1983; pp. 8-10.	☐	☐
		On-line Encyclopedia Britannica, 2001, definition of "rare-earth element.", date not established; 2 pages.	☐	☐

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Sheet 6 of 6	**Attorney Docket Number**	**14466**

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		SZE, S.M. Physics of Semiconductor Devices, John Wiley & Sons, Second Edition, 1981; pp. 293-294.	☐	☐
		CALVET, L. E., LUEBBEN, H., REED, M.A., WANG, C., SNYDER, J.P., and TUCKER, J.R. Subthreshold and scaling of PtSi Schottky barrier MOSFETs, 2000 Academic Press, *Superlattices and Microstructures*, Vol. 28, No. 5/6; pp. 501-506.	☐	☐
		WOLF, Stanley. Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET. Lattice Press, 1995; pp. 183-187.	☐	☐
		Web page "provided by Laurie Calvet", "Device Physics of the SBMOSFET", http://www.eng.yale.edu/reedlab/research/semicond.html, date not established; 7 pages.	☐	☐
		WINSTEAD, B. and RAVAIOLI, U. Simulation of Schottky Barrier MOSFET's with a Coupled Quantum Injection/Monte Carol Technique. *IEEE Transactions on Electron Device*, Vol. 47, No. 6, June 2000; pp. 1241-1246.	☐	☐
		GANG, D., XIAOYAN, L., LEI, S., JIAPING, Y., RUQI, H., HOULET, P., and FUJITAN, H. Monte Carol Simulation of 50nm n-Channel Schottky Barrier Tunneling Transistors. *Chinese Journal of Electronics*, Vol. 11, No. 2, April 2002; pp. 200-203.	☐	☐
		RISHTON, S.A., ISMAIL, K., CHU, J.O., CHAN, K.K., LEE, K.Y. New Complimentary metal-oxide semiconductor technology with self-aligned Schottky source/drain and low-resistance T gates. *J. Vac. Sci. Technol. B*, 15(6), Nov/Dec 1997, pp. 2795-2798.	☐	☐
		KEDZIERSKI, J., XUAN, P., SUBRAMANIAN, V., BOKOR, J., KING, T-J., HU, C., ANDERSON, E. A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/drain. *Superlattices and Microstructures*, Vol. 28, No. 5/6, 2000, pp. 445-452.	☐	☐
			☐	☐
			☐	☐
			☐	☐

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